Claims

1.   (Original)   An automatic test equipment (ATE) bidirectional drive channel for transmitting test signals to a device under test (DUT) and receiving signal from the DUT, comprising:

5   an input/output line for connection to a DUT, a

            driver circuit connected to apply test signals to said input/output line for application to a DUT,

            a receiver circuit connected to said input/output line to receive signals produced by a DUT, said receiver

10   circuit having an associated capacitance, and

            a first passive matching network connected to said line to at least partially compensate for said receiver circuit capacitance.

2.   (Currently Amended) The ATE drive channel of claim 1, said first passive matching ~~circuit~~ network comprising a T-coil circuit.

3.   (Original)   The ATE dive channel of claim 2, wherein said driver and receiver circuits are implemented on a common layer of an integrated circuit (IC), and said T-coil circuit includes inductors that are implemented in a

5   separate layer of said IC that is spaced from said common layer by at least a dielectric layer.

4.   (Original)   The ATE drive channel of claim 3, further comprising a flip-chip bump having an associated redistribution layer at the same level as said T-coil inductors.

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5. (Original) The ATE drive channel of claim 1, said driver circuit comprising the combination of a current-mode driver having an associated capacitance and a voltage-mode driver, said receiver circuit comprising a comparator circuit for comparing a signal received from a DUT to a reference, further comprising a second passive matching network connected in series with said first passive matching network to at least partially compensate for said current-mode driver capacitance.

6. (Currently Amended) The ATE drive channel of claim 5, said first and second passive matching ~~circuits~~ networks comprising respective T-coil circuits.

7. (Original) An automatic test equipment (ATE), receive channel for receiving signals from a device under test (DUT), comprising:

an output line for connection to a DUT,

at least one receiver circuit connected to said output line to received signals produced by a DUT, said receiver circuit having an associated capacitance, and

a passive matching network connected to said line to at least partially compensate for said receiver capacitance.

8. (Currently Amended) The ATE receive channel of claim 7, said passive matching ~~circuit~~ network comprising a T-coil circuit.

9. (Original) The ATE receive channel of claim 8, wherein said receiver circuit is implemented on one layer of an integrated circuit (IC), and said T-coil

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circuit includes inductors that are implemented in a

5 separate layer of said IC that is spaced from said first

layer by at least a dielectric layer.

10. (Original)   The ATE receive channel of claim
9, further comprising a flip-chip bump having an associated
redistribution layer at the same level as said T-coil
inductors.

11. (New)   An automatic test equipment (ATE)
bidirectional drive channel for transmitting test signals
to a device under test (DUT) and receiving signals from the
DUT, comprising:

5   an input/output line for connection to a DUT,

a driver circuit connected to apply test signals
to said input/output line for application to a DUT,

a receiver circuit connected to said input/output
line to receive signals produced by a DUT, said receiver

10 circuit having an associated capacitance, and

a first bidirectional passive matching network
connected to said line to at least partially compensate for
said receiver circuit capacitance.

12. (New)   The ATE drive channel of claim 11, said
first bidirectional passive matching network comprising a
T-coil circuit.

13. (New)   The ATE drive channel of claim 12,
wherein said driver and receiver circuits are implemented
on a common layer of an integrated circuit (IC), and said
T-coil circuit includes inductors that are implemented in a

5 separate layer on said IC that is spaced from said common layer by at least a dielectric layer.

14. (New)   The ATE drive channel of claim 13, further comprising a flip-chip bump having an associated redistribution layer at the same level as said T-coil inductors.

15. (New)   The ATE drive channel of claim 11, said driver circuit comprising the combination of a current-mode driver having an associated capacitance and a voltage-mode driver, said receiver circuit comprising a comparator
5 circuit for comparing a signal received from a DUT to a reference, further comprising a second bidirectional passive matching network connected in series with said first bidirectional passive matching network to at least partially compensate for said current-mode drive
10 capacitance.

16. (New)   The ATE drive channel of claim 15, said first and second bidirectional passive matching networks comprising respective T-coil circuits.

17. (New)   An automatic test equipment (ATE) receive channel for receiving signals from a device under test (DUT), comprising:
           an output line for connection to a DUT,
5   at least one receiver circuit connected to said output line to receive signals produced by a DUT, said receiver circuit having an associated capacitance, and

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a passive bidirectional matching network connected to said line to at least partially compensate for

10 said receiver capacitance.

18. (New)   The ATE receive channel of claim 17, said bidirectional passive matching network comprising a T-coil circuit.

19. (New)   The ATE receive channel of claim 18, wherein said receiver circuit is implemented on one layer of an integrated circuit (IC), and said T-coil circuit includes inductors that are implemented in a separate layer

5 of said IC that is spaced from said first layer by at least a dielectric layer.

20. (New)   The ATE receive channel of claim 19, further comprising a flip-chip bump having an associated redistribution layer at the same level as said T-coil inductors.